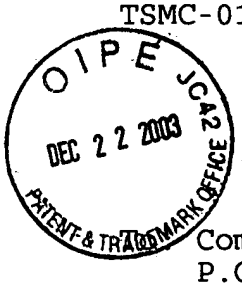
TSMC-01-037B



December 17, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/682,052 10/09/03

Kuo-Rey Peng et al.

A POLYCRYSTALLINE SILICON DIODE STRING FOR ESD PROTECTION OF DIFFERENT POWER SUPPLY CONNECTIONS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 12/19/03

U.S. Patent 6,118,155 to Voldman, "Integrated ESD Structures for Use in ESD Circuitry," discloses an ESD structure with poly between the diodes.

The paper "On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Application," by Wang et al., EOS/ESD Symposium 00-266, pp. 3A.4.1 - 3A.4.10, discloses a novel on-chip ESD protection design by using polysilicon diodes for smart card application.

The following three U.S. Patents discuss ESD device structures:

1) U.S. Patent 5,674,761 to Chang et al., "Method of Making ESD Protection Device Structure for Low Supply Voltage Applications."
2) U.S. Patent 5,856,214 to Yu, "Method of Fabricating a Low Voltage Zener-Triggered SCR for ESD Protection in Integrated Circuits."
3) U.S. Patent 6,096,584 to Ellis-Monaghan et al., "Silicon-on-Insulator and CMOS-on-SOI Double Film Fabrication Process with a Coplanar Silicon and Isolation Layer and Adding a Second Silicon Layer on One Region."

U.S. Patent 4,616,404 to Wang et al., "Method of Making Improved Lateral Polysilicon Diode by Treating Plasma Etched Sidewalls to Remove Defects," describes a method of making improved lateral polycrystalline silicon diode by treating plasma-etched sidewalls to remove defects.

U.S. Patent 6,229,157 to Sandhu, "Method of Forming a Polysilicon Diode and Devices Incorporating Such Diode," discloses a polycrystalline diode.

The following two U.S. Patents disclose a polycrystalline diode structure that has a high voltage tolerance, which is to be used for mixed-voltage, and mixed signal and analog/digital applications:

1) U.S. Patent 6,232,163 to Voldman et al., "Method of Forming a Semiconductor Diode with Depleted Polysilicon Gate Structure."
2) U.S. Patent 6,015,993 to Voldman et al., "Semiconductor Diode with Depleted Polysilicon Gate Structure and Method."

An application of polycrystalline silicon diodes is shown in "On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Process," Ker et al., IEEE Journal of Solid-State Circuits, IEEE, New York, Vol.36, No.4, April 2001, pp.678-686.

Another application describing applications using poly-crystalline silicon diodes as the ESD clamp devices in CMOS process is shown in "On-Chip ESD Protection Design for GHz RF Integrated Circuits by Using Polycrystalline Silicon Diodes in Sub-quarter-micron CMOS Process," Chang and Ker, Proceedings 2000 Electrical Overstress and Electrostatic Discharge Symposium, IEEE, New York, NY, 2000, pp. 3A 4,1 - 3A 4.10.

Another application for polycrystalline silicon diodes for ESD applications is described in "Design of the Turn-On Efficient Power-Rail ESD Clamp Circuit with Stacked Polysilicon Diodes," Ker and Chen, Proceeding of the 2001 International Symposium on Circuits and Systems, IEEE, New York, 2001, pp. IV-758-IV-761.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-037B	10/682,052
Applicant: Kou-Rey Peng et al.	
Filing Date: 10/09/03	Group Art Unit:

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6118155	9/12/00	Voldman	257	360	6/16/99
	5674761	10/7/97	Chang et al.	437	29	5/2/96
	5856214	1/5/99	Yu	438	133	3/4/96
	6096584	8/1/00	Ellis-Monaghan et al.	438	151	3/12/98
	4616404	10/14/86	Wang et al.	29	576B	11/30/84
	6229157	5/8/01	Sandhu	257	75	8/11/99
	6232163	5/15/01	Voldman et al.	438	212	7/28/99
	6015993	1/18/00	Voldman et al.	257	355	8/31/98

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

—	The paper "On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Application," by Wang et al., EOS/ESD Symposium 00-266, pp. 3A.4.1 - 3A.4.10.
—	"On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Process," Ker et al., IEEE Journal of Solid-State Circuits, IEEE, New York, Vol. 36, No. 4, April 2001, pp. 678-686.

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

"On-Chip ESD Protection Design for GHz RF Integrated Circuits by Using Polycrystalline Silicon Diodes in Sub-quarter-micron CMOS Process," Chang and Ker, Proceedings 2000 Electrical Overstress and Electrostatic Discharge Symp., IEEE, New York, NY, 2000, pp. 3A4.1-3A.4.11

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	"Design of the Turn-On Efficient Power-Rail ESD Clamp Circuit with Stacked Polysilicon Diodes," Ker and Chen, Proceeding of the 2001 Int'l Symp. on Circuits and Systems, IEEE, New York, 2001, pp. IV-758-IV-761.

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